



Applicant appreciatively acknowledges the Examiner's confirmation of receipt of Applicant's claim for priority and certified priority document under 35 U.S.C. § 119(a)-(d).

Reconsideration of the application is respectfully requested.

Claims 1 - 8 are presently pending in the application. Claims 1 - 5 have been amended. Applicant gratefully acknowledges that claim 5 has been indicated as being allowable if rewritten to include the limitations of the claim from which that claim depends.

On page 2 of the above-identified Office Action, the specification was objected to because of the following informalities: the "List of reference numbers" paragraph on page 19 should be placed before the page declaring "What is claimed" on page 15. The Examiner's suggested corrections have been made.

Also on page 2 of the Office Action, claims 1 - 5 were objected to because of various informalities. The Examiner's suggested corrections have been made.

On page 2 of the Office Action, claims 1 and 8 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U.

S. Patent No. 6,140,841 to Suh ("SUH"). On page 3 of the Office Action, claims 2 and 3 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by SUH. On page 4 of the Office Action, claims 4 and 6 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by SUH.

Applicant respectfully traverses the above rejections.

Applicant's claim 1 recites a driver stage for driving an output on one of n levels, which are each spaced from each other by a voltage difference of ΔV , comprising:

"a plurality of field effect transistors for driving the output by leading a current to or away from the output,

with the relationship of the channel widths of at least two field effect transistors, which both act either for leading current to or away from, being set in dependence on the value of the voltage difference."
[emphasis added by Applicant]

Similarly, independent claim 8 of the instant application recites a method for manufacturing a driver stage for driving an output on one of n-levels, which are each spaced from each other by a voltage difference of ΔV , comprising the following steps:

"forming a plurality of field effect transistors for driving the output by supplying or removing current to or from the output, with the relationship of the channel width of at least two field effect transistors, which both function to either lead

current to or away, being set in dependence on the value of the voltage difference." [emphasis added by Applicant]

As such, all of Applicant's claims recite, among other limitations, that "the relationship of the channel widths of at least two field effect transistors, . . . , being set in dependence on the value of the voltage difference". As stated on page 3 of the instant application, lines 16 - 28:

"The recognition of the present invention consist in that the simple scaling of the channel widths, such that the ratio of the channel widths of the respectively activated push-transistors, i. e. the respective current-supplying field effect transistors, or the respective activated pull-transistors, i.e. the respective current-removing field effect transistors, equals the ratio of the desired voltage level changes, results in errors when decoding on the receiver-side and/or in analog/digital conversion, and that instead, the ratio of the channel widths below the pull- and/or push-field effect transistors is to be adjusted depending on the desired value of the voltage difference between the desired n-output levels." [emphasis added by Applicant]

However, this is not the case with the SUH reference, cited in the Office Action. Rather, the SUH reference is already described in the instant application, page 1, line 23 - page 2, line 21. As described therein, SUH discloses that the ratios of the channel width of the field-effect transistors of a driver stage are set independently of the value of the voltage difference between the n-output levels. This can be seen clearly from Tables 1, 3, 6 and 7 of SUH, where it is shown that varying the voltage difference ΔV in SUH does not

influence the channel width ratio. In contrast to the teachings of **SUH**, Applicant's claims require, among other limitations, that the relationship of the channel width of the field-effect transistors of the driver stage are set depending on the value of the voltage difference among the n-output levels.

Page 3 of the Office Action states:

"Regarding claims 1 and 8, Figs. 2 and 6A of Suh teaches a driver stage (Fig. 6A) for driving an output on one of n levels (4 levels, Fig. 7) or a method of manufacturing a driver stage, which are each spaced from each other by a voltage difference of dV (see TABLE 6 on col. 6), comprising: a plurality of field effect transistors (MP61, 62 and MN61, 62) for driving the output by leading a current to or away from the output (see the drive current TABLE 6), with the relationship of the channel widths of at least two field effect transistors, which both act either for leading current to or away from, being set in dependence on the value of the voltage difference (different data signals creates different channel width, which translates into different voltages, channel width and voltage are dependent each other [sic], i.e. different voltages inherently requires different channel width and different channel width produces different voltages)." [emphasis added by Applicant]

Applicant respectfully disagrees with the characterization in the Office Action regarding the channel widths ("different data signals . . . different voltages"). Although the Examiner is correct in his statement that "different channel widths translate into different voltages", as indicated above, in the present case, the setting of the relationship or ratio

of the channel widths of at least two field-effect transistors

is concerned, rather than the general absolute rules regarding an individual channel width, as to which the statement in the Office Action relates. Similarly, where the Office Action states "channel width and voltage are dependent on each other" although this may be correct, the statement is not directed to a relationship between two different channel widths, as required by Applicant's claims, but focuses on a general relationship for individual channel width settings.

Applicant's believe that neither the general rules relating voltage and channel width of a single field-effect transistor, recited in the Office Action, nor any teaching in SUH, teach or suggest Applicant's particularly claimed "relationship of the channel widths of at least two field effect transistors, . . . , being set in dependence on the value of the voltage difference".

As such, Applicant believes that the present claims are patentable over the SUH reference.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1 and 8. Claims 1 and 8 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because

they all are ultimately dependent on claim 1. As it is believed that the claims were patentable over the cited art in their original form, the claims have not been amended to overcome the references.

Finally, Applicant appreciatively acknowledges the Examiner's statement that claim 5 "would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." In light of the above, Applicant respectfully believes that rewriting of claim 5 is unnecessary at this time.

In view of the foregoing, reconsideration and allowance of claims 1 - 8 are solicited.

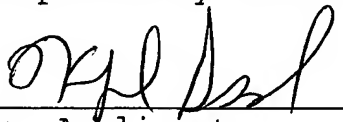
In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

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Response Dated July 19, 2005
Responsive to Office Action of April 19, 2005

Please charge any fees that might be due with respect to
Sections 1.16 and 1.17 to the Deposit Account of Lerner and
Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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